PATENT-2003

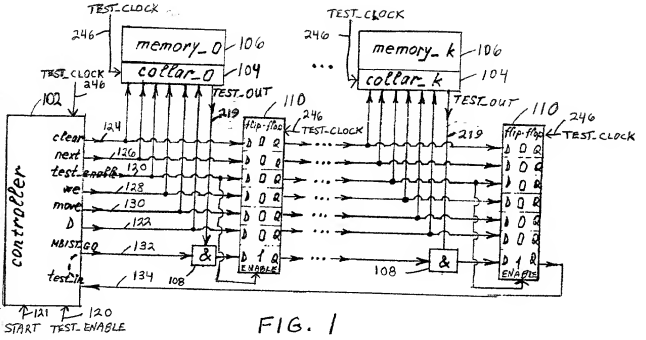

FIG. 1

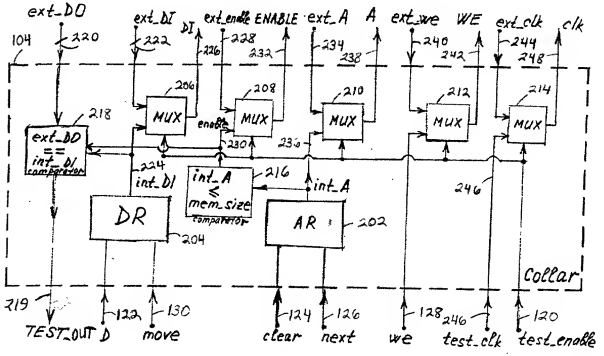

FIG. 2

TO221-11/2001

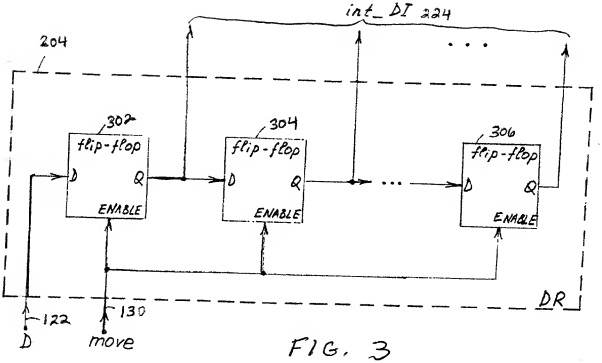

FIG. 3

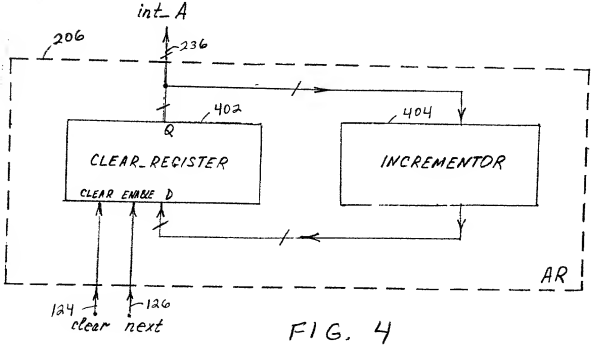

FIG. 4

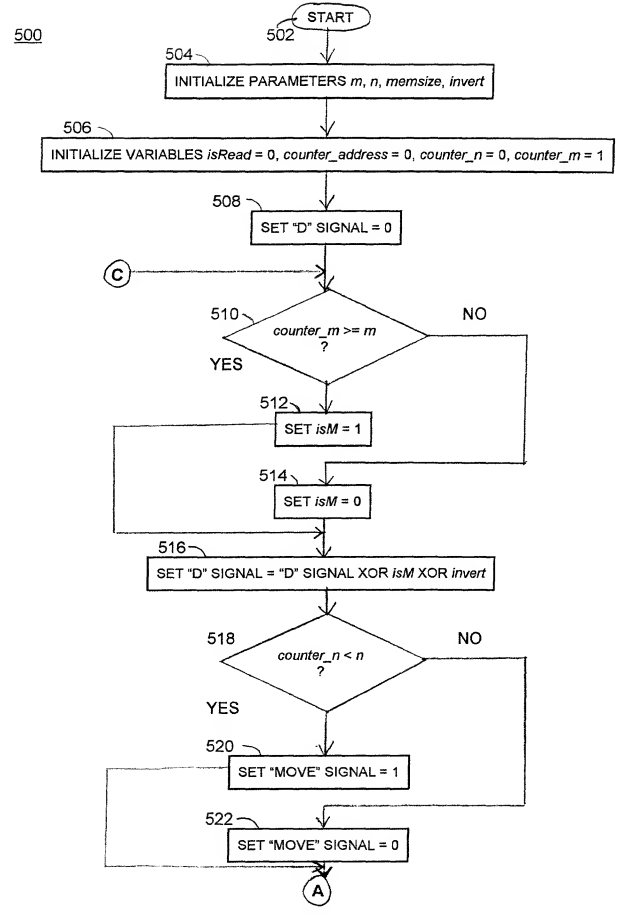
500
START
502
504
INITIALIZE PARAMETERS m, n, memsize, invert
506
INITIALIZE VARIABLES isRead = 0, counter_address = 0, counter_n = 0, counter_m = 1
508
SET "D" SIGNAL = 0
C
510
counter_m >= m ?
NO
YES
512
SET isM = 1
514
SET isM = 0
516
SET "D" SIGNAL = "D" SIGNAL XOR isM XOR invert
518
counter_n < n ?
NO
YES
520
SET "MOVE" SIGNAL = 1
522
SET "MOVE" SIGNAL = 0
A

FIG. 5A

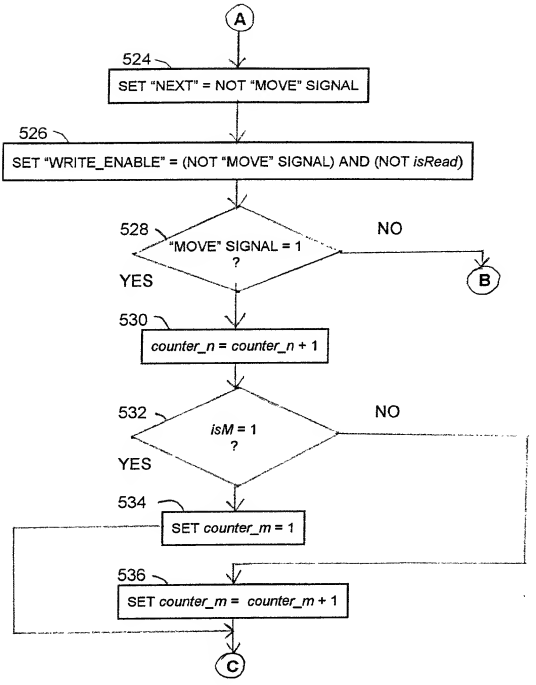
A
524
SET "NEXT" = NOT "MOVE" SIGNAL
526
SET "WRITE_ENABLE" = (NOT "MOVE" SIGNAL) AND (NOT isRead)
528
"MOVE" SIGNAL = 1
?
NO
B
YES
530
counter_n = counter_n + 1
532
isM = 1
?
NO
YES
534
SET counter_m = 1
536
SET counter_m = counter_m + 1
C

FIG. 5B

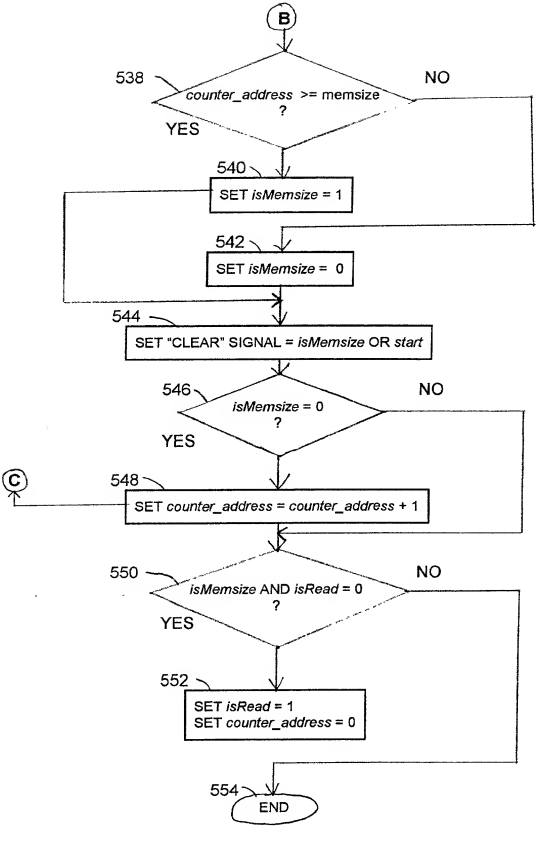
B
538
counter_address >= memsize
?
NO
YES
540
SET isMemsize = 1
542
SET isMemsize = 0
544
SET "CLEAR" SIGNAL = isMemsize OR start
546
isMemsize = 0
?
NO
YES
C
548
SET counter_address = counter_address + 1
550
isMemsize AND isRead = 0
?
NO
YES
552
SET isRead = 1
SET counter_address = 0
554
END

FIG. 5C

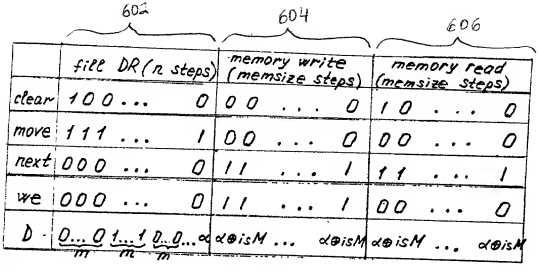
602
604
606
fill DR (n steps)
memory write (memsize steps)
memory read (memsize steps)
clear
move
next
we
D
100 ... 0
00 ... 0
10 ... 0
111 ... 1
00 ... 0
00 ... 0
000 ... 0
11 ... 1
11 ... 1
000 ... 0
11 ... 1
00 ... 0
0...0 1...1 0...0 α
α⊕isM ... α⊕isM
α⊕isM ... α⊕isM
m
m
m

FIG. 6

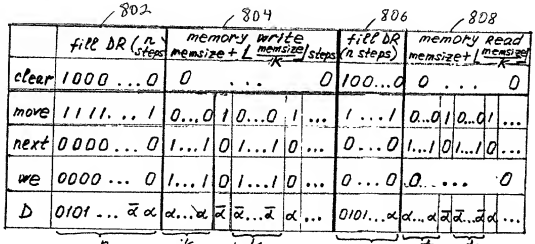
802
804
806
808
fill DR (n steps)
memory write
memsize + L
memsize/k steps
fill DR (n steps)
memory read
memsize + L
memsize/k
clear
move
next
we
D
1000 ... 0
0 ... 0
100...0
0 ... 0
1111. .. 1
0...0 1 0...0 1 ...
1 ... 1
0...0 1 0...0 1 ...
0000 ... 0
1...1 0 1...1 0 ...
0 ... 0
1...1 0 1...1 0 ...
0000 ... 0
1...1 0 1...1 0 ...
0 ... 0
0 ... 0
0101 ... α̅ α
α...α α̅ α̅...α̅ α ...
0101...α
α...α α̅ α̅...α̅ α ...
n
k
k
n
k
k

FIG. 8

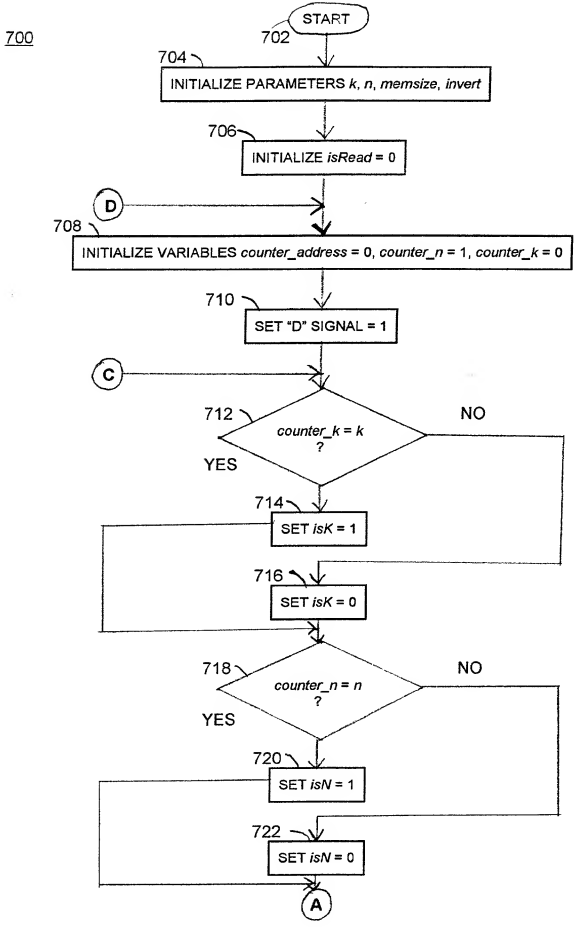
700
START
702
704
INITIALIZE PARAMETERS k, n, memsize, invert
706
INITIALIZE isRead = 0
D
708
INITIALIZE VARIABLES counter_address = 0, counter_n = 1, counter_k = 0
710
SET "D" SIGNAL = 1
C
712
counter_k = k ?
NO
YES
714
SET isK = 1
716
SET isK = 0
718
counter_n = n ?
NO
YES
720
SET isN = 1
722
SET isN = 0
A

FIG. 7A

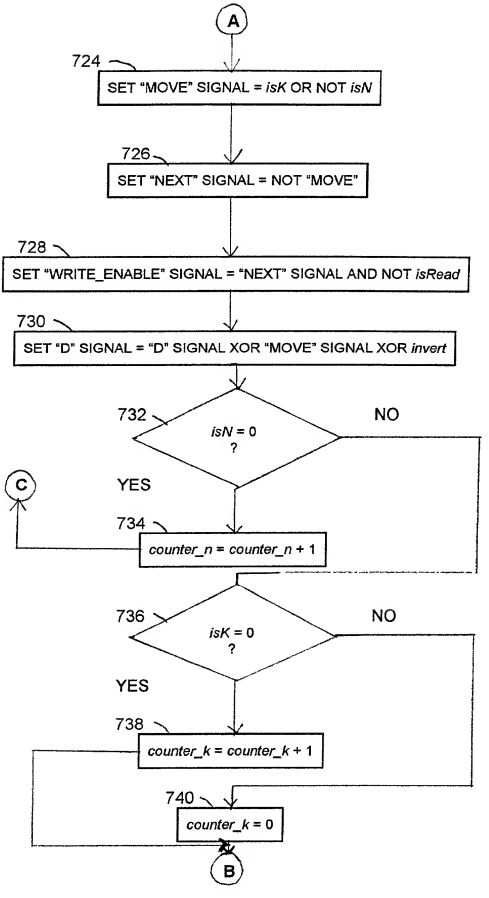
A
724
SET "MOVE" SIGNAL = isK OR NOT isN
726
SET "NEXT" SIGNAL = NOT "MOVE"
728
SET "WRITE_ENABLE" SIGNAL = "NEXT" SIGNAL AND NOT isRead
730
SET "D" SIGNAL = "D" SIGNAL XOR "MOVE" SIGNAL XOR invert
732
isN = 0 ?
NO
YES
C
734
counter_n = counter_n + 1
736
isK = 0 ?
NO
YES
738
counter_k = counter_k + 1
740
counter_k = 0
B

FIG. 7B

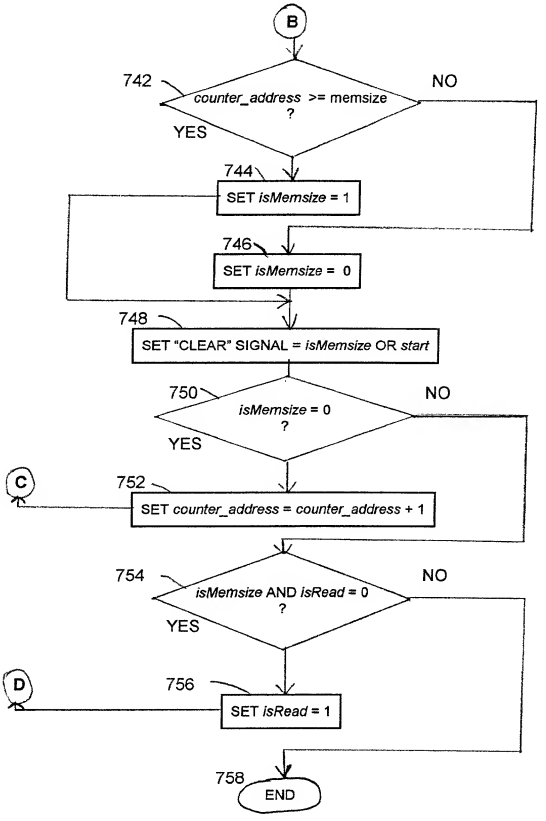
B
742
counter_address >= memsize ?
NO
YES
744
SET isMemsize = 1
746
SET isMemsize = 0
748
SET "CLEAR" SIGNAL = isMemsize OR start
750
isMemsize = 0 ?
NO
YES
C
752
SET counter_address = counter_address + 1
754
isMemsize AND isRead = 0 ?
NO
YES
D
756
SET isRead = 1
758
END

FIG. 7C